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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/748,077	12/22/2000	Andrew Cofler	S1022/8583	3246

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EXAMINER

MEONSKE, TONIA L

ART UNIT	PAPER NUMBER
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2183

DATE MAILED: 01/28/2005

14

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/748,077

Applicant(s)

COFLER ET AL.

Examiner

Tonia L Meonske

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 September 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 17, 19, 22, and 24 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Alpert et al., US Patent 5,621,886.

3. The rejections are respectfully maintained and incorporated by reference as set forth in the last office, paper number 7, action mailed on February 14, 2004.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1, 3, 4, 5, 6, 7, 8, 9, 11, 12, 13, 14, 15, 16, 18, 20, 21, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karp et al., US Patent 5,748,936, in view of Alpert et al., US Patent 5,621,886.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Karp et al., US Patent 5,748,936, in view of Alpert et al., US Patent 5,621,886, and Page, Reconfigurable Processors, Oxford University Hardware Compilation Group Invited Keynote Address for Heathrow PLD Conference.

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7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Karp et al., US Patent 5,748,936, in view of Alpert et al., US Patent 5,621,886, and Swoboda, US Patent 5,828,824.

8. The rejections are respectfully maintained and incorporated by reference as set forth in the last office, paper number 7, action mailed on February 14, 2004.

Response to Arguments

9. Applicant's arguments filed June 23, 2004 have been fully considered but they are not persuasive.

10. On page 3, Applicant argues in essence:

“Alpert does not disclose or suggest suspending processor execution based on a stall signal or a stall attribute associated with debug instructions.”

However, Alpert has taught suspending processor execution based on a stall attribute associated with debug instructions. When the processor is operating in a debug mode, or a breakpoint mode, the status register bits indicate as such and processor execution is suspended, either on a branch event or on an address event (column 6). This suspension is based on the status registers, or stall attributes, associated with the debug instruction.

Therefore this argument is moot.

11. On page 4, Applicant argues in essence:

“Nowhere does Alpert disclose or suggest a stall attribute associated with a debug instruction and a decode unit that includes stall control circuitry which is responsive to reading of the stall attribute. As discussed above, Alpert teaches that processor execution is suspended upon recognition of an address breakpoint or branch breakpoint. This is different from placing a decode unit into a stall state based upon reading a stall attribute that is associated with a debug instruction.”

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However, Alpert has taught a stall attribute associated with a debug instruction and a decode unit that includes stall control circuitry which is responsive to reading of the stall attribute. In Alpert, the status registers are the stall attributes (column 6). On a break address event or a break branch event, the entire pipeline is stalled, including the decode stage for debugging (See Figure 4, and columns 11 and 12.). Therefore, Alpert has in fact taught a stall attribute associated with a debug instruction (status registers) and a decode unit that includes stall control circuitry which is responsive to reading of the stall attribute (When the status registers are read to indicate an active debug mode, the pipeline, including the decode stage, is stalled for debugging. See Figure 4, and columns 11 and 12.). Therefore this argument is moot.

12. On page 5, Applicant argues in essence:

“Alpert discloses that execution of a processor is suspended based upon recognition of an event, but does not teach or suggest that the stall state of a computer system is set by reading stall attributes associated with debug instructions in a debug mode.”

However, the status registers in Alpert are read to set, or activate, the debug mode instructions (column 6). Alpert has in fact taught that the stall state of the computer system is set by reading stall attributes, or status registers, associated with debug instructions in a debug mode. Therefore this argument.

13. On page 6, Applicant argues in essence:

“One of ordinary skill in the art would not have been motivated to combine Karp and Alpert, as the two references relate to entirely different technical fields. Specifically, Karp is directed to speculative execution in a processor. Alpert is directed towards the unrelated field of performing debugging during execution of instructions by a processor.”

However, the fact that Karp et al. and Alpert et al. may be two different concepts is irrelevant. Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Karp et al. has been cited for teaching predicated instructions. Karp et al. has not specifically taught the single-stepping debugging. Alpert has taught the claimed single-stepping debugging, for the desirable purpose of providing the programmer with valuable tool for looking at the dynamic state of the processor after each instruction (Alpert et al., column 1, lines 27-36, column 1, line 65-column 2, line 4). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Karp et al., include the claimed single-stepping of Alpert et al., for the desirable purpose of providing the programmer with valuable tool for looking at the dynamic state of the processor after each instruction (Alpert et al., column 1, lines 27-36, column 1, line 65-column 2, line 4). Therefore this argument is moot.

14. On page 7, Applicant argues in essence:

"The office action asserts that Alpert discloses executing a divert routine for each committed instruction and executing the next instruction in the instruction sequence for each non-committed instruction. Applicants respectfully disagree with this assertion. Alpert does not disclose executing a divert routine for each committed instruction. Alpert teaches executing a debug handler routine only upon recognition of an event, such as an address breakpoint or branch breakpoint (Col. 2, lines 41-48). Executing a divert routine for each committed instruction is different from executing a debug handler based on recognition of an event. ... That is, Alpert does not disclose or suggest that only some

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instructions in the instruction sequence are to be executed. Therefore, Alpert does not disclose or suggest non-committed instructions. While some instructions in the instruction sequence may not trigger a debug routine (i.e., due to the programmer disabling certain types of events), these instructions are nevertheless committed for execution."

However, the fact that Alpert et al. may not disclose or suggest that only some instructions in the instruction sequence are to be executed is irrelevant as Karp et al. has been cited or this teaching. In Karp, instructions that are not committed are not of interest to the programmer as non-committed instruction do not changed the architectural state of the processor. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Karp et al., include the claimed emulation unit, as taught by Alpert et al., for the desirable purpose of providing the programmer with valuable tools for looking at the dynamic state of the processor after each committed instruction (Alpert et al., column 1, lines 27-36, column 1, line 65-column 2, line 4). Therefore this argument is moot.

15. On page 8, Applicant argues in essence:

"As should be clear from the discussion above, neither Alpert nor Karp, taken alone or in combination, discloses or suggests, "an emulation unit including control circuitry which cooperates with the decode unit to selectively control the decode unit to implement step-by-step execution of an instruction sequence wherein, for each committed instruction, a divert routine is executed by the computer system and for each non-committed instruction the next instruction in the instruction sequence is executed," as recited in claim 1. "

...

"As should be clear from the discussion above, neither Alpert nor Karp, taken alone or in combination, discloses or suggests, "if the instruction is committed, implementing a divert routine whereby debug code is executed and, if the instruction is not committed, fetching and decoding the next instruction in the instruction sequence," as recited in claim 13. "

However, Karp et al. in combination with Alpert et al. have taught an emulation unit including control circuitry which cooperates with the decode unit to selectively control

the decode unit to implement step-by-step execution of an instruction sequence wherein, for each committed instruction, a divert routine is executed by the computer system and for each non-committed instruction the next instruction in the instruction sequence is executed, as recited in claim 1 and similarly in claim 13. Karp et al. have not taught that for each committed instruction, a divert routine is executed by the computer system and for each noncommitted instruction the next instruction in the instruction sequence is executed. However, Alpert et al. have taught for each committed instruction, a divert routine is executed (Alpert et al., Figure 3, elements 2, 4, and 6, column 12, lines 59-65). Furthermore, Alpert et al. have taught disabling debug breakpoints when they are not of interest to the programmer in order to improve the system performance (Alpert et al., column 9, lines 40-column 10, line 6). Instructions that are not committed are not of interest to the programmer as non-committed instructions do not change the architectural state of the processor. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Karp et al., include for each committed instruction, executing a divert routine, as taught by Alpert et al., (Alpert et al., Figure 3, elements 2, 4, and 6, column 12, lines 59-65) and for each noncommitted instruction the next instruction in the instruction sequence is executed, for the desirable purpose of disabling unnecessary debug breakpoints in order to improve system performance (Alpert et al., column 9, lines 40-column 10, line 6). Therefore, we arrived at the claimed invention with the obvious combination of the concepts of Karp et al. and Alpert et al. Therefore this argument is moot.

Conclusion

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16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

17. A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, 8-4:30.

19. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

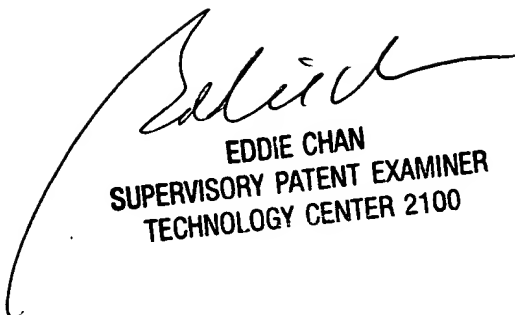
20. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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